# Aaditya Gaur

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Computer Engineering undergraduate specializing in **ASIC Design**, **FPGA hardware design**, and **Embedded Systems**. Proven experience in architecting SystemVerilog SoCs with standard bus protocols and developing bare-metal firmware for microprocessor peripherals. Skilled in bridging the hardware-software gap to build optimized, high-performance systems.

## EDUCATION

**Purdue University**, West Lafayette, IN *May 2027*
Bachelor of Science in Computer Engineering
*GPA: 3.75/4.0*
*Relevant Coursework:* ASIC Design, Microprocessor Systems, Algorithmic Analysis, Data Structures, Signals & Systems
*Honors:* Garmin Scholar, Dean's List & Semester Honors

## TECHNICAL SKILLS

**Hardware Design (RTL):** SystemVerilog, Verilog, VHDL, QuestaSim, Xilinx Vivado
**Embedded Systems:** C, C++, ARM Cortex-M, RISC-V, STM32, Raspberry Pi
**Protocols & Peripherals:** UART, I2C, SPI, USB, PWM, AMBA, ADCs/DACs, GPIO, Timers, FIFO
**Programming & Tools:** Python, MATLAB, Git, Linux, KiCAD, Analog Discovery

## TECHNICAL PROJECTS

**Custom SoC Architecture & RTL Design** — *SystemVerilog, AHB/APB, QuestaSim*
- Architecting a modular SystemVerilog SoC with **AHB and APB bus fabrics** connecting custom peripheral IP.
- Designed and verified a **UART receiver** and **FIR hardware accelerator**, optimized for timing closure and area.
- Implemented a **USB 1.1 controller** including endpoint buffers, packet decoding, and transaction management.
- Built layered testbenches in QuestaSim to validate protocol compliance and ensure deterministic behavior.

**AlgoFPGA: Hardware Algorithm Accelerator Library** — *Vivado, Verilog, RTL*
- Developing a reproducible FPGA accelerator library implementing hardware versions of key algorithms.
- Created fully-parameterized RTL blocks for algorithmic primitives, enabling fast prototyping and collaborative extension.
- Built timing-optimized implementations using Xilinx Vivado and validated functionality using simulation testbenches.

**MAJA: Embedded Motion-Controlled Console** — *C, RP2350, SPI/I2C, PCB Design*
- Programmed low-level C drivers for TFT display (SPI) and IMU (I2C) on the RP2350 MCU.
- Designed a custom PCB integrating the TFT display, keypad, IMU sensor, and RP2350 controller into a single compact board.

**BoilerVibe: Social App for Purdue Students** — *UI/UX, Frontend Development*
- Designed a responsive UI and implemented core front-end features to ensure smooth user experience across devices.
- Optimized interface transitions and navigation to improve usability and engagement.

## PROFESSIONAL EXPERIENCE

**Machine Learning Intern** May – Aug 2025
*CLAN Labs, Purdue University* Remote
- Worked with Prof. Vaneet Agarwal on atmospheric turbulence optimization for astronomical imaging systems.
- Implemented reinforcement learning pipelines using **Proximal Policy Optimization (PPO)** to iteratively correct extreme turbulence without relying on wavefront sensors.
- Built Bayesian Neural Networks to validate RL models, improving reliability, quantifying uncertainty, and ensuring robustness across varying turbulence conditions.

**Undergraduate Teaching Assistant** Aug 2024 – Present
*Purdue ECE (ECE 368, ECE 369, ENGR 131)* West Lafayette, IN
- Supported instruction for 200+ students, simplifying complex algorithmic and logic concepts into simple explanations.
- Delivered weekly office hours and personalized guidance, strengthening students' problem-solving ability and foundational reasoning essential for embedded and hardware design.

**ML Researcher** May – Aug 2024
*Laboratory for Computational Social Systems (LCS2), IIT Delhi* New Delhi, India
- Analyzed 500+ annotated internet memes to investigate bias propagation in Large Language Models under Prof. Tanmoy Chakraborty.
- Applied statistical and algorithmic techniques to characterize harmful content bias and identify model failure modes.